CLAIMS

I claim:

1. A method of forming a structure on a substrate, the method comprising:

a) depositing a first dielectric layer on the substrate;

b) depositing a second dielectric layer on the first dielectric layer, wherein the first and second dielectric layers have dissimilar etching characteristics;

c) depositing a third dielectric layer on the second dielectric layer;

d) depositing a fourth dielectric layer on the third dielectric layer, wherein the first and fourth dielectric layers have dissimilar etching characteristics;

e) depositing a fifth dielectric layer on the fourth dielectric layer, wherein the fifth dielectric layer has dissimilar etching characteristics with regard to the second and the fourth dielectric layers, and wherein the first and fifth dielectric layers have similar etching characteristics;

f) simultaneously anisotropically etching a power line trench and a via pattern through the fifth, fourth and third dielectric layers, in a first etching sequence; and

g) anisotropically etching a signal line trench, overlaying the via pattern, through the fifth dielectric layer, and anisotropically etching the via pattern to the substrate thereby forming a first via hole extending from the signal line trench to the substrate, in a second etching sequence, wherein the power line trench and the signal trench having an underlying via hole are adapted for forming a triple damascene structure.

2. The method of claim 1 wherein the first etching sequence comprises:

a) forming a mask layer, having a power line trench pattern and the via pattern, on the fifth dielectric layer;

b) anisotropically etching the power line trench pattern through the fifth, fourth and third dielectric layers, thereby forming a power line trench and simultaneously anisotropically etching the via pattern through the fifth, fourth and third dielectric layers; and

c) removing the mask layer.

3. The method of claim 1 wherein the second etching sequence comprises:

a) forming a mask layer, having a signal line trench pattern overlaying the via pattern, on the fifth dielectric layer and forming the mask layer inside the power line trench;

b) anisotropically etching the via pattern through the second dielectric layer; and

c) anisotropically etching the signal line trench pattern through the fifth dielectric layer thereby forming a signal line trench, and simultaneously anisotropically etching the via pattern through the first dielectric layer.

4. The method of claim 1 wherein the first, third and fifth dielectric layers comprise one or more dielectric materials selected from the group consisting of amorphous fluorinated carbon, organic spin-on materials, spin-on-glass, aero-gel, poly(arylene) ethers, fluorinated poly(arylene) ethers and divinyl siloxane benzocyclobutane.

5. The method of claim 4 wherein the second and fourth dielectric layers comprise one or more dielectric materials selected from the group consisting of SiO_2 and fluorinated SiO_2.

6. The method of claim 1 wherein the first, third and fifth dielectric layers comprise one or more dielectric materials selected from the group consisting of SiO_2 and fluorinated SiO_2.

7. The method of claim 6 wherein the second and fourth dielectric layers comprise one or more dielectric materials selected from the group consisting of amorphous fluorinated carbon, organic spin-on materials, spin-on-glass, aero-gel, poly(arylene) ethers, fluorinated poly(arylene) ethers and divinyl siloxane benzocyclobutane.

8. The method of claim 1 additionally comprising simultaneously filling the power line trench, the signal line trench and the first via hole with a conductive material, whereby a triple damascene structure is formed.

9. The method of claim 8 wherein the conductive material comprises one or more

materials selected from the group consisting of metals, alloys, metallic superconductors and nonmetallic superconductors.

10. The method of claim 1 additionally comprising forming a second via hole underlying the power line trench and extending to the substrate, wherein the power line trench, the signal line trench, and the first and second via holes are adapted for forming a quadruple damascene structure.

11. The method of claim 10 additionally comprising simultaneously filling the power line trench, the signal line trench, the first via hole and the second via hole with a conductive material, whereby a quadruple damascene structure is formed.

12. A method of forming a structure on a substrate, the method comprising:

a) depositing a cap layer on the substrate;

b) depositing a first dielectric layer on the cap layer;

c) depositing a second dielectric layer on the first dielectric layer, wherein the first and second dielectric layers have dissimilar etching characteristics;

d) depositing a third dielectric layer on the second dielectric layer;

e) depositing a fourth dielectric layer on the third dielectric layer, wherein the first and fourth dielectric layers have dissimilar etching characteristics, and wherein the cap layer and the second and fourth dielectric layers have similar etching characteristics;

f) depositing a fifth dielectric layer on the fourth dielectric layer, wherein the fifth dielectric layer has dissimilar etching characteristics with regard to the cap layer and to the second and the fourth dielectric layers, and wherein the first and fifth dielectric layers have similar etching characteristics;

g) simultaneously anisotropically etching a power line trench pattern and a via pattern through the fifth, fourth and third dielectric layers, in a first etching sequence; and

h) anisotropically etching a signal line trench, overlaying the via pattern, through the fifth and fourth dielectric layers, anisotropically etching the via pattern to the substrate thereby forming a first via hole extending from the signal line trench to the substrate, and anisotropically etching the power line trench pattern through the

second dielectric layer thereby forming a power line trench, in a second etching sequence.

13. The method of claim 12 wherein the first etching sequence comprises:

a) forming a mask layer, having the power line trench pattern and the via pattern, on the fifth dielectric layer;

b) anisotropically etching the power line trench pattern through the fifth, fourth and third dielectric layers, and simultaneously anisotropically etching the via pattern through the fifth, fourth and third dielectric layers; and

c) removing the mask layer.

14. The method of claim 12 wherein the second etching sequence comprises:

a) forming a mask layer, having a signal line trench pattern overlaying the via pattern, on the fifth dielectric layer and forming the mask layer inside the power line trench;

b) anisotropically etching the via pattern through the second dielectric layer;

c) anisotropically etching the signal line trench pattern through the fifth dielectric layer thereby forming a signal line trench, and simultaneously anisotropically etching the via pattern through the first dielectric layer; and

d) anisotropically etching the signal line trench pattern through the fourth dielectric layer, simultaneously anisotropically etching the power line trench pattern through the second dielectric layer and simultaneously anisotropically etching the via pattern through the cap layer.

15. The method of claim 12 additionally comprising simultaneously filling the power line trench, the signal line trench and the first via hole with a conductive material, whereby a triple damascene structure is formed.

16. The method of claim 12 additionally comprising forming a second via hole, underlying the power line trench, extending to the substrate.

17. The method of claim 16 additionally comprising simultaneously filling the power line trench, the signal line trench, the first via hole and the second via hole with a conductive

material, whereby a quadruple damascene structure is formed.

18. A method of forming a structure on a substrate, the method comprising:

a) depositing a first dielectric layer on the substrate;

b) depositing a second dielectric layer on the first dielectric layer, wherein the first and second dielectric layers have dissimilar etching characteristics;

c) depositing a third dielectric layer on the second dielectric layer, wherein the second and third dielectric layers have dissimilar etching characteristics and wherein the first and third dielectric layers have similar etching characteristics;

d) simultaneously anisotropically etching a power line trench and a via pattern through the third and second dielectric layers, in a first etching sequence; and

e) anisotropically etching a signal line trench, overlaying the via pattern, through the third dielectric layer, and simultaneously etching the via pattern to the substrate thereby forming a first via hole extending from the signal line trench to the substrate, in a second etching sequence.

19. The method of claim 18 wherein the first etching sequence comprises:

a) forming a mask layer, having a power line trench pattern and the via pattern, on the third dielectric layer;

b) anisotropically etching the power line trench pattern through the third and second dielectric layers, thereby forming a power line trench and simultaneously anisotropically etching the via pattern through the third and second dielectric layers; and

c) removing the mask layer.

20. The method of claim 18 wherein the second etching sequence comprises:

a) forming a mask layer, having a signal line trench pattern overlaying the via pattern, on the third dielectric layer and forming the mask layer inside the power line trench, and;

b) anisotropically etching the signal line trench pattern through the third dielectric layer thereby forming a signal line trench, and simultaneously anisotropically etching the via pattern through the first dielectric layer.

21. The method of claim 18 wherein the first and third dielectric layers comprise one or more dielectric materials selected from the group consisting of amorphous fluorinated carbon, organic spin-on materials, spin-on-glass, aero-gel, poly(arylene) ethers, fluorinated poly(arylene) ethers and divinyl siloxane benzocyclobutane.

22. The method of claim 21 wherein the second dielectric layer comprises one or more dielectric materials selected from the group consisting of SiO_2 and fluorinated SiO_2.

23. The method of claim 18 additionally comprising simultaneously filling the power line trench, the signal line trench and the first via hole with a conductive material, whereby a triple damascene structure is formed.

24. The method of claim 18 additionally comprising forming a second via hole, underlying the power line trench, extending to the substrate.

25. The method of claim 24 additionally comprising simultaneously filling the power line trench, the signal line trench, the first via hole and the second via hole with a conductive material, whereby a quadruple damascene structure is formed.

26. A method of forming a structure on a substrate, the method comprising:

a) depositing a first dielectric layer on the substrate;

b) depositing a second dielectric layer on the first dielectric layer;

c) depositing a third dielectric layer on the second dielectric layer, wherein the first, second and third dielectric layers have similar etching characteristics;

d) simultaneously anisotropically etching a power line trench pattern and a via pattern through the third and second dielectric layers, in a first etching sequence; and

e) anisotropically etching a signal line trench, overlaying the via pattern, through the third dielectric layer, and simultaneously anisotropically etching the via pattern to the substrate thereby forming a first via hole extending from the signal line trench to the substrate, in a second etching sequence.

27. The method of claim 26 wherein the first etching sequence comprises:

a) forming a mask layer, having the power line trench pattern and the via pattern, on the third dielectric layer;

b) timed anisotropically etching the power line trench pattern through the third and second dielectric layers, thereby forming a power line trench and simultaneously timed anisotropically etching the via pattern through the third and second dielectric layers; and

c) removing the mask layer.

28. The method of claim 26 wherein the second etching sequence comprises:

a) forming a mask layer, having a signal line trench pattern overlaying the via pattern, on the third dielectric layer and forming the mask layer inside the power line trench; and

b) timed anisotropically etching the signal line trench pattern through the third dielectric layer thereby forming a signal line trench, and simultaneously timed anisotropically etching the via pattern through the first dielectric layer.

29. The method of claim 26 wherein the first, second and third dielectric layers comprise one or more dielectric materials selected from the group consisting of SiO_2 and fluorinated SiO_2.

30. The method of claim 26 additionally comprising simultaneously filling the power line trench, the signal line trench and the first via hole with a conductive material, whereby a triple damascene structure is formed.

31. The method of claim 26 additionally comprising forming a second via hole, underlying the power line trench, extending to the substrate.

32. The method of claim 31 additionally comprising simultaneously filling the power line trench, the signal line trench, the first via hole and the second via hole with a conductive material, whereby a quadruple damascene structure is formed.

33. A device comprising:

a) a substrate;

b) a first dielectric layer positioned on the substrate;

c) a second dielectric layer positioned on the first dielectric layer, wherein the first and second dielectric layers have dissimilar etching characteristics;

d) a third dielectric layer positioned on the second dielectric layer;

e) a fourth dielectric layer positioned on the third dielectric layer, wherein the first and fourth dielectric layers have dissimilar etching characteristics;

f) a fifth dielectric layer positioned on the fourth dielectric layer, wherein the fifth dielectric layer has dissimilar etching characteristics with regard to the second and the fourth dielectric layers, and wherein the first and fifth dielectric layers have similar etching characteristics;

g) a first region in the fifth dielectric layer defining a power line trench extending through the fifth, fourth and third dielectric layers;

h) a second region in the fifth dielectric layer defining a signal line trench extending through the fifth dielectric layer; and

i) a third region in the fourth dielectric layer underlying the signal line trench, defining a via hole extending through the fourth, third, second and first dielectric layers, wherein the power line trench, the signal line trench and the via hole are adapted for containing a triple damascene structure.

34. An apparatus for controlling the formation of a fabricated structure on a substrate, the apparatus comprising:

a) at least one controller adapted for interacting with a plurality of fabrication stations including: (1) a first fabrication station for depositing a first dielectric layer on a substrate, (2) a second fabrication station for depositing a second dielectric layer on the first dielectric layer, (3) a third fabrication station for depositing a third dielectric layer on the second dielectric layer, (4) a fourth fabrication station for depositing a fourth dielectric layer on the third dielectric layer, (5) a fifth fabrication station for depositing a fifth dielectric layer on the fourth dielectric layer, (6) a sixth fabrication station for simultaneously anisotropically etching a power line trench pattern and a via pattern through the fifth, fourth and third dielectric layers, and (7) a seventh fabrication station for anisotropically etching a signal line trench pattern through the fifth dielectric layer and anisotropically etching the via pattern through the second and first dielectric layers; and

b) a data structure which causes the controller to control the formation of the fabricated structure.